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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

GOUDREAU, GEORGE A

ART UNIT	PAPER NUMBER
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1763

DATE MAILED: 01/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

08-846671

Applicant(s)

Ko

Examiner

George Goudreau

Group Art Unit

1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- ☒ Responsive to communication(s) filed on 9-01-10 to 11-01-11 (i.e., papers # 20-22).
- ☐ This action is FINAL.
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- ☒ Claim(s) 1-10, 12-14, 16-20, 24-38, 40-44, 46, 50-52, 54-58 is/are pending in the application.
- Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- ☒ Claim(s) 1-10, 12-14, 16-20, 24-38, 40-44, 46, 50-52, 54-58 is/are rejected.
- ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- ☐ Claim(s) \_\_\_\_\_ are subject to restriction or election requirement

## Application Papers

- ☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).
- ☐ All ☐ Some\* ☐ None of the:
- ☐ Certified copies of the priority documents have been received.
- ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

\*Certified copies not received: \_\_\_\_\_

## Attachment(s)

- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2, 22
- ☒ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Interview Summary, PTO-413
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Other \_\_\_\_\_

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15. This action will not be made final due to the new grounds of rejection.
16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claims 1-10, 12-14, 16-20, 24-38, 40-44, 46, 50-52, and 54-58 are rejected under 35

U.S.C. 103(a) as being unpatentable over Sadjadi et. al. (5,883,436).

Sadjadi et. al. disclose a process for forming a SAC between 2 gates on a CZ-Si wafer which is comprised of the following steps:

- Polysil gates (201) which have a SiO<sub>2</sub> cap (209), and which are on top of a SiO<sub>2</sub> pad layer are formed onto the surface of a CZ-Si wafer (100).;
- SiO<sub>2</sub> sidewall spacers (204) are formed onto the sides of the polysil gates.;
- A ILD dielectric layer (205) which is comprised of any of BPSG, PSG, and BSG is used to planarize the surface of the wafer.;
- A patterned photo resist etch mask is formed onto the surface of the ILD (205).;
- A SAC (206) is etched through the ILD (205) down to the surface of the CZ-Si wafer while maintaining an etch selectivity relative to the SiO<sub>2</sub> cap layer (209), and the SiO<sub>2</sub> sidewall spacers (204) using a plasma which is comprised of CF<sub>4</sub>-CHF<sub>3</sub>-N<sub>2</sub>-Ar.

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This is shown specifically in figures 2 a-2 e; and is shown in general in figures 1-3. This is discussed specifically in columns 5-7; and is discussed in general in columns 1-10. Sadjadi et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

- the specific usage of the type of plasma etcher which is claimed by the applicant;
- the specific formation of a conductive plug in the SAC formed between the gates on the wafer in the process taught above;
- the specific usage of a plasma comprised of either  $\text{CH}_2\text{F}_2$  or  $\text{CH}_3\text{F}$  to selectively etched the doped oxide layer to the undoped oxide layer in the process taught above;
- the specific formation of the gates on the wafer out of W polycide; and
- the specific etch process parameters which are claimed by the applicant

It would have been obvious to one skilled in the art to employ any of a variety of different type of plasma etchers in the etching process taught above including those which are specifically claimed by the applicant. The usage of these types of plasma etchers to conduct a plasma etching process is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, the specific usage of these types of plasma etchers to conduct the etching process taught above would have simply involved the usage of alternative, and at least equivalent means for conducting the plasma etching process taught above to the usage of other means for conducting the plasma etching process.

It would have been obvious to one skilled in the art to form a conductive plug in the SAC opening formed in the ILD layer in the region between adjacent gates in the process taught above

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based upon the following. The formation of a conductive plug in a SAC contact located between adjacent gates on a wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, it would have been desirable to provide some means for electrically connecting circuitry formed above the ILD layer in the process taught above to the SAC region of the wafer using a conductive material such as a plug in the SAC.

It would have been obvious to one skilled in the art to employ a plasma comprised of either  $\text{CH}_2\text{F}_2$  or  $\text{CH}_3\text{F}$  to selectively etch the doped oxide layer to the undoped oxide layer in the process taught above based upon the following. The usage of a plasma comprised of either  $\text{CH}_2\text{F}_2$  or  $\text{CH}_3\text{F}$  to selectively etch a doped oxide layer to an undoped oxide layer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, the usage of a plasma comprised of either  $\text{CH}_2\text{F}_2$  or  $\text{CH}_3\text{F}$  to selectively etch a doped oxide layer to an undoped oxide layer in the process taught above simply represents the usage of an alternative, and at least equivalent means for conducting this etching step in the process taught above to those means which are specifically taught above.

It would have been obvious to one skilled in the art to fabricate the gates on the wafer out of W polycide in the process taught above based upon the following. The formation of gates on a wafer out of W polycide is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, the specific formation of gates on the semiconductor wafer in the process taught above out of W polycide simply represents the

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usage of an alternative, and at least equivalent means for forming the gate on the semiconductor wafer in the process taught above to the usage of other means for forming the gate.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching processes taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etch process parameters which are claimed by the applicant are result effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

18. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

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19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

  
George A. Goudreau/gag

Primary Examiner

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